Production-Run Failures Diagnosis for Concurrency Bugs

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Different aspects of fighting bugs

In-house bug detection

In-field failure recovery

In-field failure diagnosis

In-house bug fixing

Low overhead

High accuracy

High accuracy

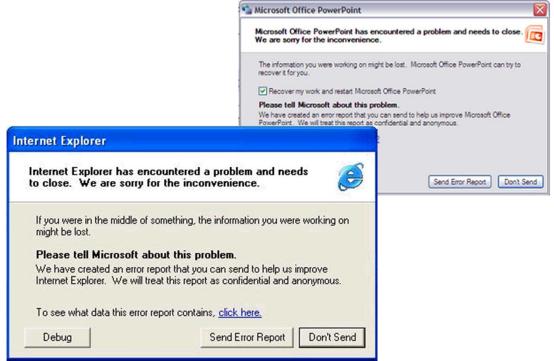


ideally, this should be a cycle, but \dots Shan Lu, 2014-1-7 SL41



Failure diagnosis is challenging

- Limited information
- Failures are difficult to repeat
- Root causes are difficult to reason about





Slide 3

if i have time, i can turn these into developers quotes $\mbox{\sc Shan Lu, }2014\mbox{-}1\mbox{-}15$ **SL35**

Example



Slide 4

i need to replace this with Joy's version Administratr, 2014-3-5 A15

Example

```
InitState(...){
     table = New();
     if (table == NULL) {
          ReportOutOfMemory();
          return JS_FALSE;
ReportOutOfMemory(){
 error("out of memory");
```

***.js out of memory



```
CALL STACK

ReportOutofMemory()

InitState()

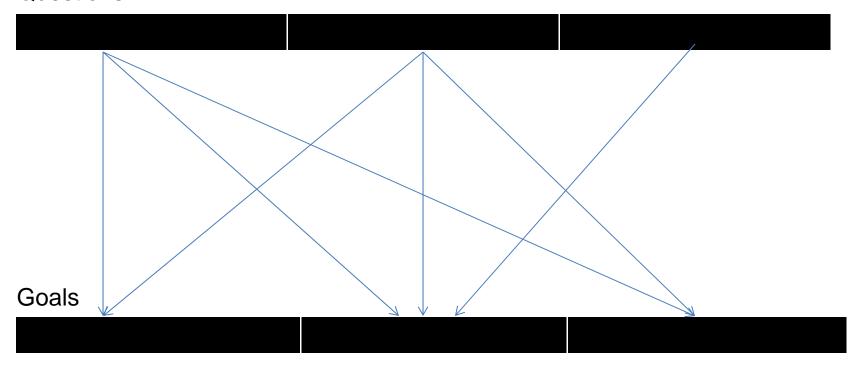
...

main()
```



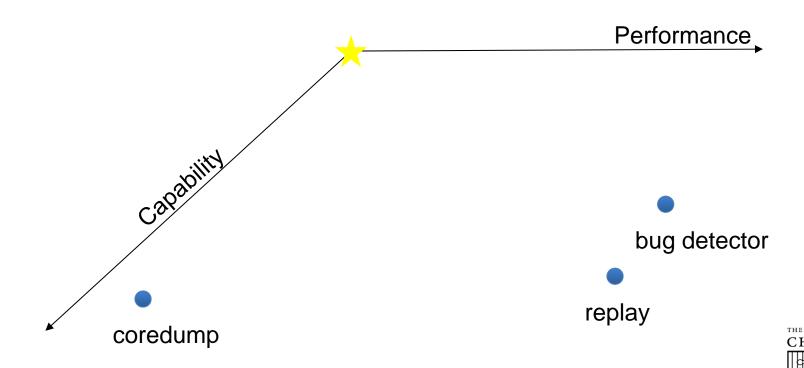
Design space

Questions

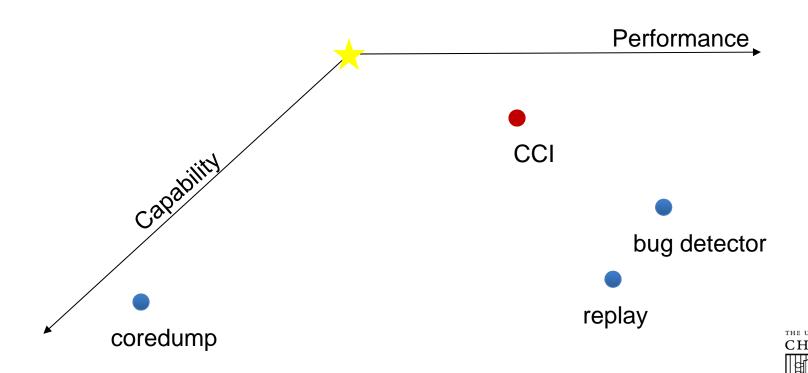




Previous work



Our work



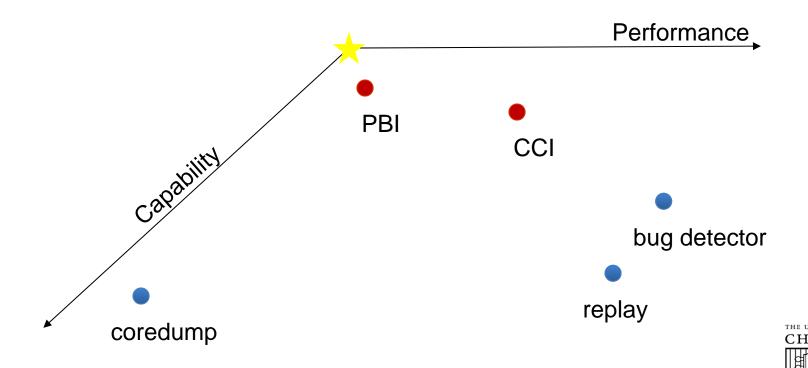
Slide 8

A14 simplify these. put

statistical approach, compiler, cause-pattern hardware support hardware extension, effect-pattern in one text box, keep growing.

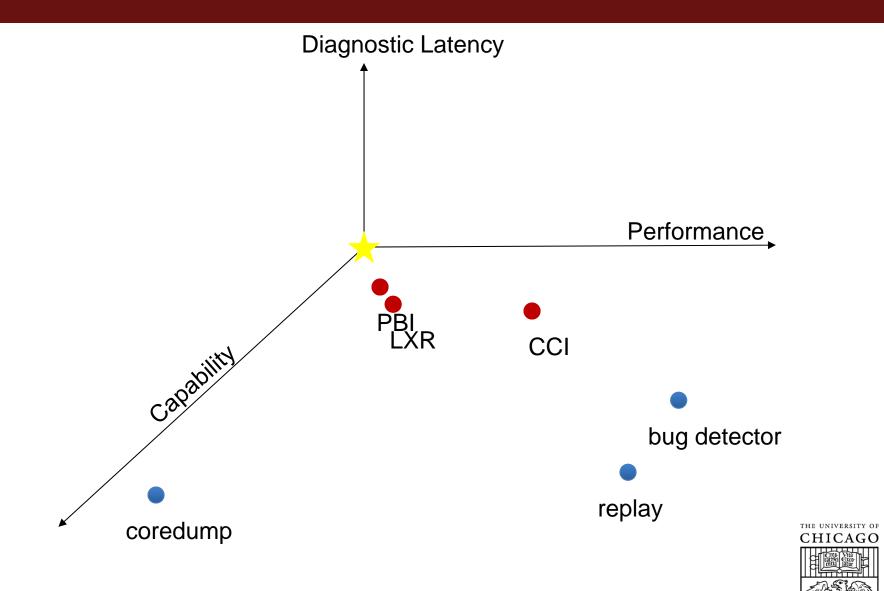
change the cloud shape. simplify both the slide and the script Administratr, 2014-3-4

Our work



SL31 maybe i should put 4-d/3-d coordinates here, and change the tables following Shan Lu, 2014-1-15

Our work

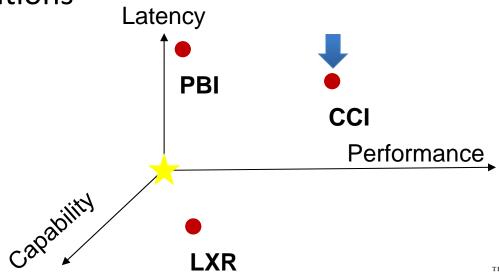


SL31 maybe i should put 4-d/3-d coordinates here, and change the tables following Shan Lu, 2014-1-15

SL33

Outline

- Overview
- Production-run failure diagnosis
 - What is the problem
 - What are our solutions



Conclusion



change the bullets texts. things like "compiler-based" is strange. $\mbox{\it Shan Lu, }$ 2014-1-15 SL33

How to do better than state-of-art?

What to collect	How to collect	How to use the collected

Performance Capability Latency



How to do better than state-of-art?

What to collect	How to collect	How to use the collected
	Sampling	

Performance Capability Latency



How to do better than state-of-art?

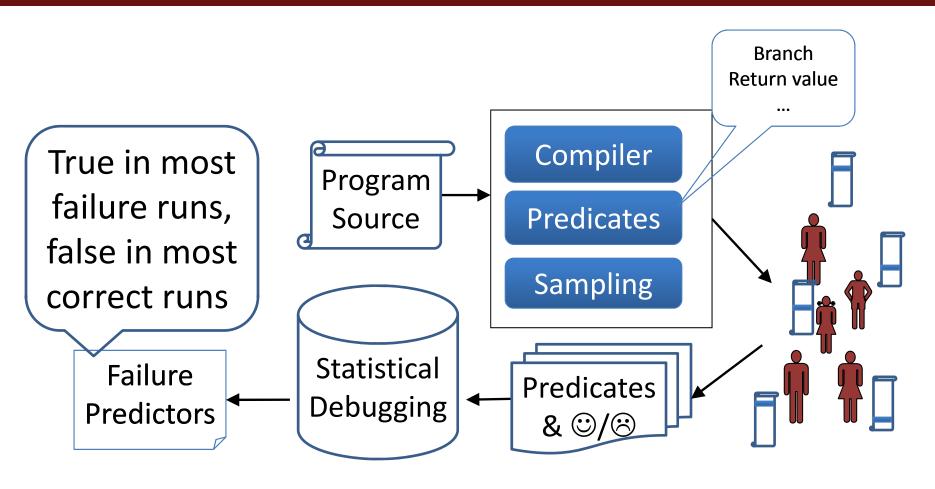
What to collect	How to collect	How to use the collected
	Sampling	Cooperative statistical analysis

Performance Capability Latency



Cooperative Bug Isolation (CBI)

SI 20



Performance	Capability
Good	??



Slide 15

SL20 do i need to provide a sequential bug diagnosis example?
 Shan Lu, 2014-1-10

 SL34 should i add an overview slide before this saying: challenges; solutions: apply xxx to concurrency bug diagnosis.
 Shan Lu, 2014-1-15

A long story about CBI

Statistical fault localization, delta debugging

Sampling based statistical fault localization



An example

```
1 // Print_tokens2 v7
2 if(ch == '\n')
3   return (TRUE);
4 else if(ch == ' ')
5 // Bug: should return FALSE
6   return (TRUE);
7 else
8   return (FALSE);
```



Another example

```
152
      void
      more_arrays ()
153
154
        int indx:
155
        int old_count:
156
        bc_var_array **old_ary;
157
        char **old_names;
158
159
        /* Save the old values. */
160
        old_count = a_count;
161
        old_ary = arrays;
162
        old_names = a_names;
163
164
        /* Increment by a fixed amount and allocate. */
165
        a_count += STORE_INCR;
166
        arrays = (bc_var_array **) bc_malloc (a_count*si...
167
        a names = (char **) bc_malloc (a_count*sizeof(ch...
168
169
        /* Copy the old arrays. */
170
        for (indx = 1; indx < old_count; indx++)
171
          arrays[indx] = old_ary[indx];
172
173
174
        /* Initialize the new elements. */
175
        for (; indx < v_count; indx++)
176
          arrays[indx] = NULL;
177
178
        /* Free the old elements. */
179
        if (old_count != 0)
180
181
             free (old_arv);
             free (old_names);
183
184
185
```



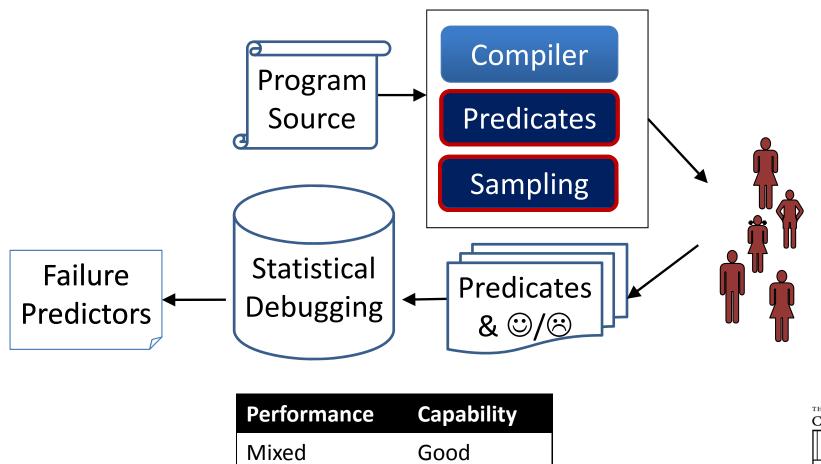
Does it work for concurrency bugs?

```
Thread 1 Thread 2

ptr = malloc(SIZE);
... free(ptr);
if (!ptr){ //b
    ReportOutofMem();
    exit(1);
}
```

Predicate
...
takenb
!takenb
...

Cooperative Con-Bug Isolation (CCI)







What to collect? (predicate design)



SL42 i need to redraw this to be consistent with earlier ...

Shan Lu, 2014-1-16

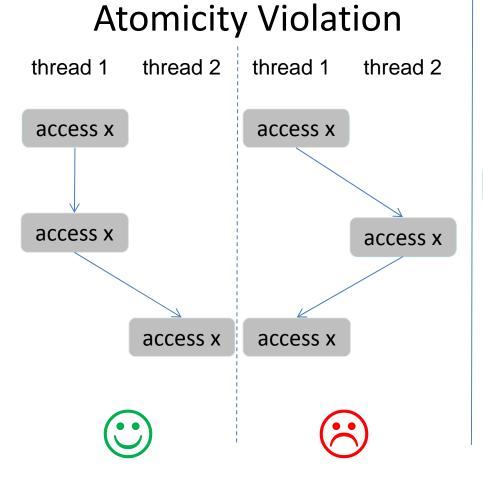
Concurrency bug root cause patterns

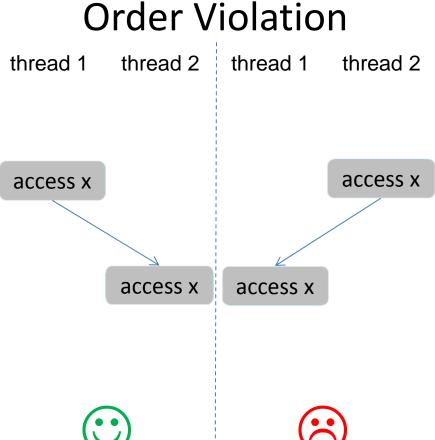
Atomicity Violation

Order Violation



Concurrency bug root cause patterns





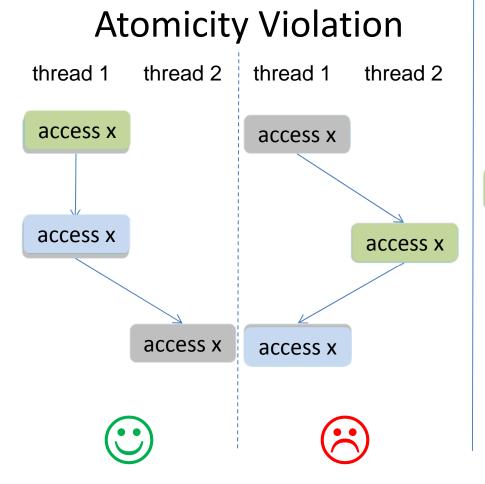


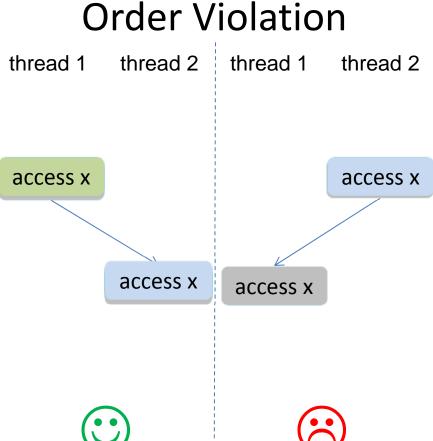
CCI-Prev predicate

Whether two successive accesses to a memory location were by two distinct threads or one thread



CCI-Prev can reflect root causes







Is CCI-Prev useful? (Example)

```
Thread 1 Thread 2

ptr = malloc(SIZE);
... free(ptr);
if (!ptr){ ptr=NULL;
    ReportOutofMem();
    exit(1);
}

Mozilla
```



Example (correct runs)

thread 1

...

free (ptr);

ptr=NULL;

...

ptr = malloc (SIZE);

if (!ptr) {

exit(1);

ReportOutofMem();

Predicate	©	8
•••		
remote _l	0	0
local _ı	1	0
•••		





Example (failure run)

```
thread 1
                                 thread 2
ptr = malloc (SIZE);
                                 free (ptr);
                                 ptr=NULL;
if (!ptr) {
  ReportOutofMem();
  exit(1);
```

Predicate	©	8
•••		
remote _l	0	1
local _ı	1	0

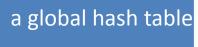




How to evaluate?

```
thread 1
                                     thread 2
   ptr = malloc (SIZE);
                                     free (ptr);
                                     ptr=NULL;
lock(glock);
remote = test_and_insert(& ptr, curTid);
record(I, remote);
temp = ptr;
unlock(glock);
if (!temp) {
 ReportOutofMem();
 exit(1);
```

Predicate	©	8
•••		
remote _l	0	1
local _ı	1	0
•••		



address	ThreadID
•••	
& ptr	1
•••	•••



How to sample?



How to sample branch predicates?

```
A: if (!temp2) {
     if (sample())
       record (A, TRUE);
   } else {
     if (sample())
                                                    B: if (!temp3) {
       record (A, FALSE);
                                                         if (sample())
                                                           record (C, TRUE);
                   independent
                                                       } else ·
B: if (!temp) {
                                                         if (sample())
     if (sample())
                                                           record (C, FALSE);
       record (B, TRUE);
                                      independent
    else {
     if (sample())
       record (B, FALSE); 4
```

How to sample CCI-Prev?

```
thread 1
                                                thread 2
ptr = malloc (SIZE);
                                                free (ptr);
                                                ptr=NULL;
if (!ptr) {
  ReportOutofMem();
  exit(1);
```



How to sample CCI-Prev?

```
thread 1
                                                       thread 2
if (sample())
lock (..);
                                                      if (sample())
                                                      lock (..);
ptr = tmp1;
unlock(...);
                                                       tmp2 = ptr;
else ...
                                                      unlock(...);
                                                      else ...
             cannot be
             independent
                                                      if (sample())
                                                      lock (..);
                              cannot be
                              independent
                                                      ptr=NULL;
unlock(...);
 if (sample())
 lock (..);
                                                      else ...
 tmp3 = ptr;
 unlock(...);
 else ...
                                       Does traditional sampling work?
```

NO!

Thread-coordinated, bursty sampling

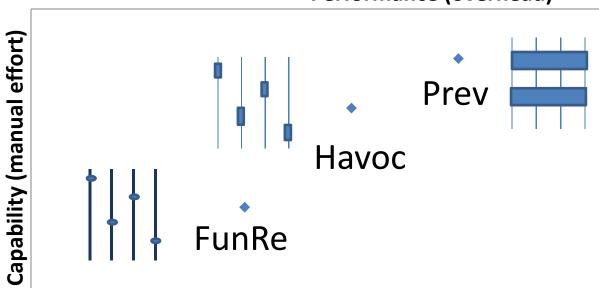
thread 1 thread 2

```
if (sample())
loc
```



Other predicates

Performance (overhead)





Evaluation methodology

Program

Apache-1

Apache-2

Cherokee

FFT

LU

Mozilla-JS-1

Mozilla-JS-2

Mozilla-JS-3

PBZIP2

CIL-based static code instrumentor 1/100 sampling rate, ~3000 runs in total (failure:success~1:1)



Diagnosis capability (w/ sampling)

Program	CCI-Prev
Apache-1	✓ top1
Apache-2	✓ top1
Cherokee	*
FFT	✓ top1
LU	✓ top1
Mozilla-JS-1	×
Mozilla-JS-2	✓ top1
Mozilla-JS-3	✓ top2
PBZIP2	✓ top1

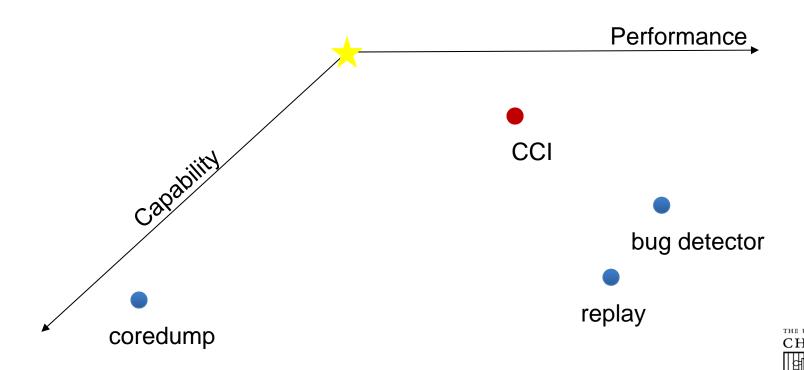


Diagnosis performance (overhead)

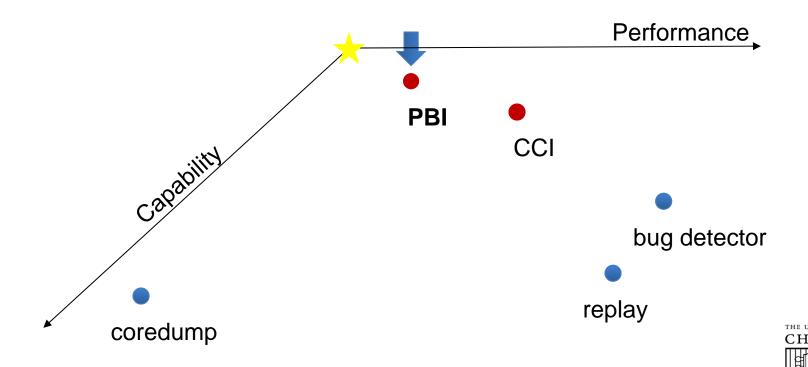
	Prev		
	No Sampling	Sampling	
Apache-1	62.6%	1.9%	
Apache-2	8.4%	0.5%	
Cherokee	19.1%	0.3%	
FFT	169 %	24.0%	
LU	57857 %	949 %	
Mozilla-JS	11311 %	606 %	
PBZIP2	0.2%	0.2%	



Are we done?



Outline



change the bullets texts. things like "compiler-based" is strange. $\mbox{\it Shan Lu, }$ 2014-1-15 SL33

What to collect	How to collect	How to use the collected
CCI-Prev	Sampling	Cooperative statistical
•••		analysis

Performance Capability Latency



What to collect	How to collect	How to use the collected
	Sampling	

Slow sampling infrastructure

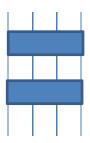


Performance Capability Latency



What to collect	How to collect	How to use the collected
	Sampling	

Slow sampling infrastructure Inaccurate evaluation



Performance Capability Latency



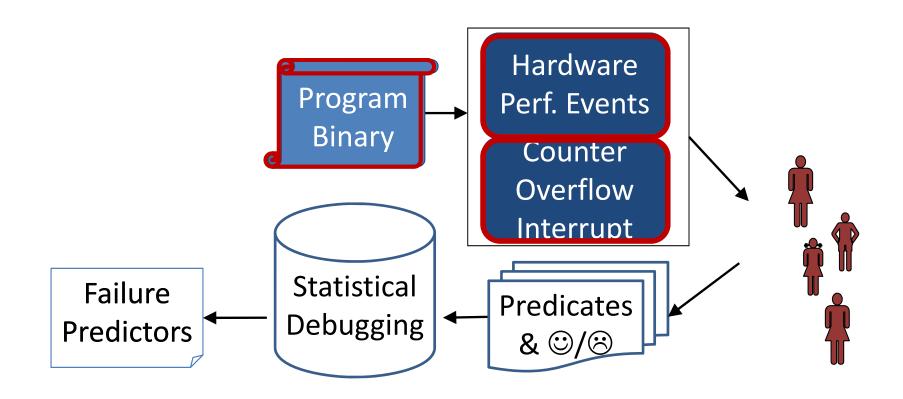
What to collect	How to collect	How to use the collected
	Hardware-based evaluation & sampling	
	Now sampling infrastructur	^



Performance	Capability	Latency
-------------	------------	---------



PerfCnt-based Bug Isolation (PBI)



Performance	Capability	Code Size	Change Hard	
Good (<5% overhead)	Good	No Change	NO!	
				JAVIII SAILL

should i bring in secret sauce here? Shan Lu, 2014-1-16 **SL38**

Hardware Performance Counters

- Registers monitor hardware performance events
 - -1-8 registers per core
 - Each register can contain an event count
 - Large collection of hardware events
 - Instructions retired, TLB misses, cache misses, etc.
- Traditional usage
 - Hardware testing/profiling

THE UNIVERSIT

What to collect?

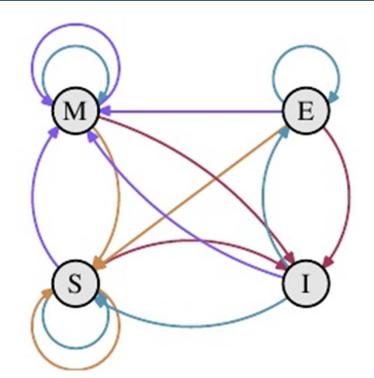


Which event can reflect root causes?

L1 data cache cache-coherence events

It tracks which cache-coherence state (M/E/S/I) an instruction observes

Modified
Exclusive
Shared
Invalid



Local read
Local write
Remote read
Remote write



Is cache-coherence event useful?

```
Thread 1 Thread 2

ptr = malloc(SIZE);
... free(ptr);
if (!ptr){ ptr=NULL;
    ReportOutofMem();
    exit(1);
}

Mozilla
```



Example (correct runs)

```
thread 1 (core 1)
```

thread 2 (core 2)

Modified

Invalid

```
free (ptr);
ptr=NULL;
```

```
ptr = malloc (SIZE);
...
I: if (!ptr) {
    ReportOutofMem();
    exit(1);
}
```

Predicate	©	8
M _I	1	0
E _I	0	0
Sı	0	0
lı	0	0





Example (failure run)

```
thread 1 (core 1)
```

Invalid

pt

```
ptr = malloc (SIZE);
```

```
thread 2 (core 2)
```

Modified

```
free (ptr);
ptr=NULL;
```

. . .

•••
if (! ptr) {
ReportOutofMem();
exit(1);
1

Predicate	©	8
•••		
M _I	1	0
E _I	0	0
Sı	0	0
li .	0	1





Useful for Atomicity Violations

Bug Type	FAILURE PREDICTOR
WWR Violation	INVALID
RWR Violation	INVALID
RWW Violation	INVALID
WRW Violation	SHARED



Useful for order violations

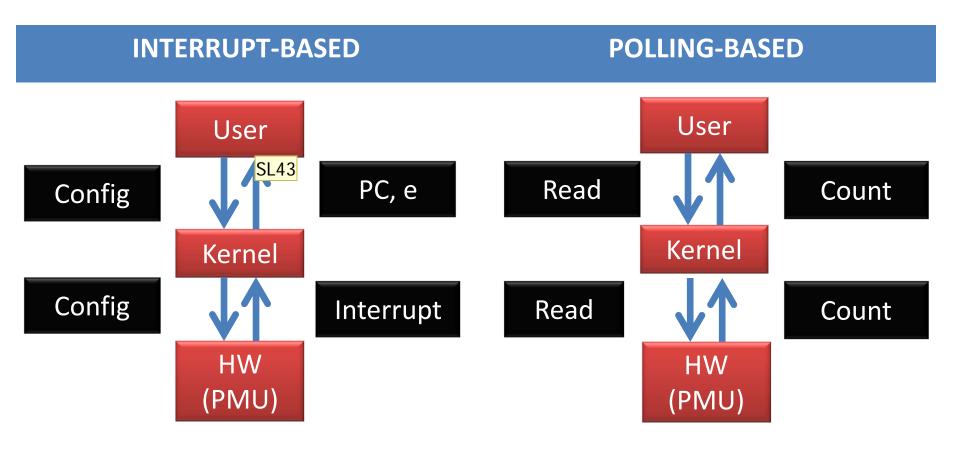
Bug Type	FAILURE PREDICTOR
Read-too-early	EXCLUSIVE (!INVALID)
Read-too-late	INVALID



How to evaluate & sample?

Which performance events occur at a specific instruction?

Accessing performance counters







double check if polling needs to go through kernel Shan Lu, 2014-1-16 SL43

More details of counter access

Log Id	APP	Core	Performance Event	Instruction	Function
1	Httpd	2	0x140 (Invalid)	401c3b	decrement _refcnt



Beyond concurrency bugs

- Which event?
 - Branch taken/non-taken event

- How to evaluate & sample?
 - Performance counter overflow interrupt



PBI vs. CBI/CCI (Qualitative)

Performance Sample in this region? Sample in this region? Are other threads sampling? Are other threads sampling? **PBI CBI**

- Diagnostic capability
 - Discontinuous monitoring (CCI/CBI)
 - Continuous monitoring (PBI)
 - PBI differentiates interleaving reads from writes



Evaluation methodology

Program

Apache-1

Apache-2

Cherokee

FFT

LU

Mozilla-JS-1

Mozilla-JS-2

Mozilla-JS-3

MySQL-1

MySQL-2

PBZIP2



Diagnosis capability (w/ sampling)

Program	CCI-Prev
Apache-1	✓ top1
Apache-2	✓ top1
Cherokee	*
FFT	✓ top1
LU	✓ top1
Mozilla-JS-1	*
Mozilla-JS-2	✓ top1
Mozilla-JS-3	✓ top2
MySQL-1	-
MySQL-2	-
PBZIP2	✓ top1



Diagnosis capability (w/ sampling)

Program	CCI-Prev	PBI
Apache-1	✓ top1	√ top1
Apache-2	✓ top1	✓ top1
Cherokee	×	✓ top1
FFT	✓ top1	√ top1
LU	✓ top1	✓ top1
Mozilla-JS-1	×	✓ top1
Mozilla-JS-2	✓ top1	✓ top1
Mozilla-JS-3	✓ top2	√ top1
MySQL-1	-	✓ top1
MySQL-2	-	✓ top1
PBZIP2	✓ top1	✓ top1



Diagnosis capability (w/ sampling)

Program	CCI-Prev	PBI
Apache-1	✓ top1	✓ top1-I
Apache-2	✓ top1	✓ top1-I
Cherokee	×	✓ top1-I
FFT	✓ top1	✓ top1-E
LU	✓ top1	✓ top1-E
Mozilla-JS-1	×	✓ top1-I
Mozilla-JS-2	✓ top1	✓ top1-I
Mozilla-JS-3	✓ top2	✓ top1-I
MySQL-1	-	✓ top1-S
MySQL-2	-	✓ top1-S
PBZIP2	✓ top1	✓ top1-I

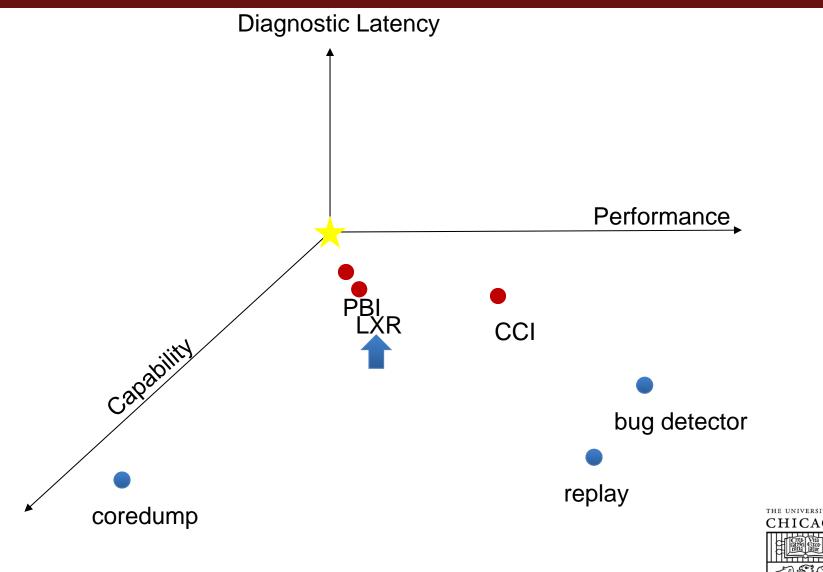


Diagnosis performance (overhead)

Program	CCI-Prev	PBI
Apache-1	1.90%	0.40%
Apache-2	0.40%	0.40%
Cherokee	0.00%	0.50%
FFT	121%	1.00%
LU	285%	0.80%
Mozilla-JS-1	800%	1.50%
Mozilla-JS-2	432%	1.20%
Mozilla-JS-3	969%	0.60%
MySQL-1	-	3.80%
MySQL-2	-	1.20%
PBZIP2	1.40%	8.40%



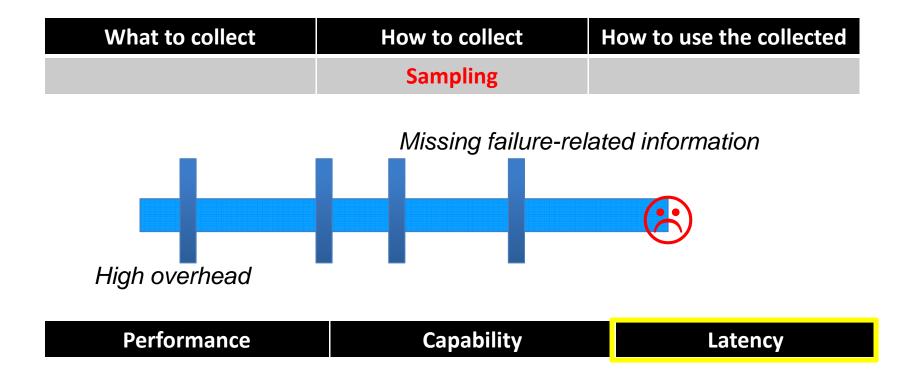
Are we done?



1/100 sampling rate → ~100 failures required for diagnosis

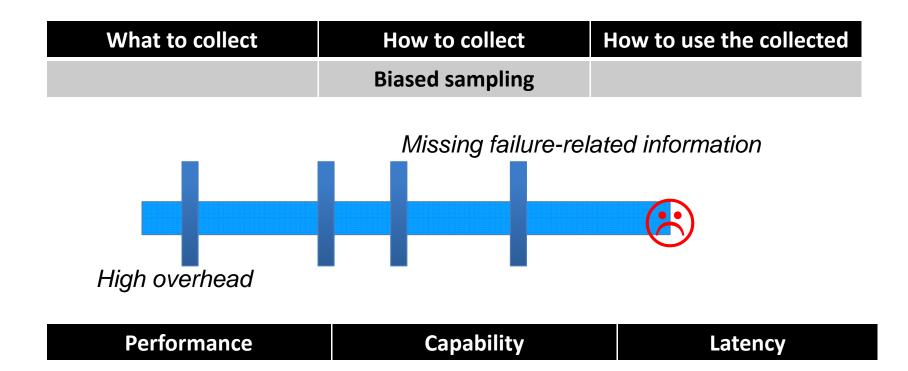
SL31 maybe i should put 4-d/3-d coordinates here, and change the tables following Shan Lu, 2014-1-15

How to do better than PBI?





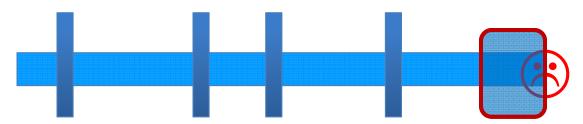
How to do better than PBI?





LXR — Last eXecution Record

- What to collect?
 - Last few branches right before failure
 - Last few cache-coherence events right before failures
- How to collect/maintain LXR?
 - Existing* hardware support!



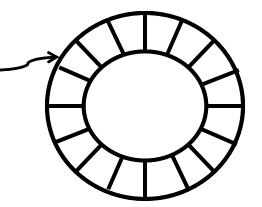
Performance	Capability	Code Size	Change Hardware?	Diagnosis Latency
Good (<5% overhead)	Good	Little Change	Simple Extension*	Short

Last Branch Record (LBR)

- Existing hardware feature
 - Store recently taken branches
 - Circular buffer with 16 entries (Intel Nehalem)
 - Negligible overhead

Branch Source Instruction Pointer

Branch Target
Instruction
Pointer

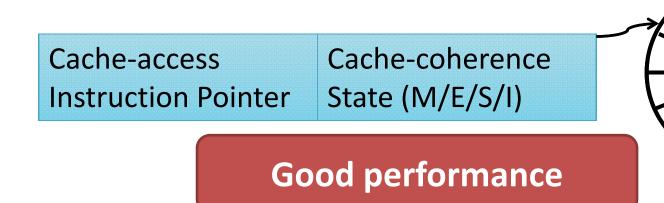


Good performance



Last Cache-coherence Record (LCR)

- Existing hardware feature
 - Configurable cache-coherence event counting
- Extension
 - Buffer to collect this information
 - Set of recent L1 data cache access instructions
- Negligible overhead (estimated)



Is LXR useful?

```
Thread 1

ptr = malloc(SIZE);
...

if (!ptr){
    ReportOutofMem();
    exit(1);
}

Apache
```

```
Thread 1 Thread 2

print("%u", End);
print("%u", End-Start);
End=time();

FFT
```

Bugs have short error-propagation distance



LXR is sufficient for failure diagnosis

Good diagnosis capability



LXR vs PBI vs CBI/CCI

	Performance	Capability	Diagnosis Latency (#-failure-runs)
LXR	<5%	23/31	1~10 failures
PBI	<5%	25/31	1000 failures
CBI/C CI	3% ~ 969%	18/31	1000 failures



Summary

